

## CLAIMS

1. A method for controlling data communications between an external interface and at least first and second chips, the first chip having a first universal asynchronous receiver-transmitters (UART), a first microcontroller, and a switching mechanism capable of connecting the first UART and the first microcontroller, and the second chip having a second microcontroller and a second UART connecting the second microcontroller to the first UART, the method comprising:
  - 10 monitoring signals communicated to the first chip from at least one of the external interface and the second UART; and
  - communicating data between the external interface and the second microcontroller via the first and second UARTs, in response to the switching mechanism detecting a predetermined signal.
- 15 2. The method of claim 1, wherein the predetermined signal is a switch sequence received from at least one of the second UART and the external interface.
- 20 3. The method of claim 1, further comprising:
  - communicating data between the external interface and the first microcontroller, after the switching mechanism has detected that a time-out period has expired.
- 25 4. The method of claim 1, wherein the switching mechanism is implemented as control software executing over the first microcontroller.
5. A method for controlling data communications between an external interface connected in series to a plurality of chips, the method comprising:

monitoring signals communicated to a first chip from at least one of the external interface and a second chip from the plurality of chips, wherein the first chip is connected between the external interface and the second chip; and  
5 communicating data between the external interface and the second chip via the first chip, in response to a switching mechanism in the first chip detecting a predetermined signal.

6. A method for controlling data communications between an external interface and at least first and second microcontrollers, wherein the first  
10 microcontroller is connectable to first and second universal asynchronous receiver-transmitters (UARTs), via a switch mechanism, and wherein the second microcontroller is respectively connected to a third UART, the method comprising:

communicating signals from the external interface to the first UART,  
15 wherein a switch mechanism monitors the signals for a predetermined signal; and  
routing data from the external interface to the second microcontroller via the first, second and third UARTs, in response to the switch mechanism detecting the predetermined signal.

20 7. The method of claim 6, further comprising:  
rerouting data from the external interface to the first microcontroller via the first UART, in response to the switch mechanism detecting the predetermined signal.

25 8. The method of claim 7, wherein the switch mechanism is implemented as control software executable on the first microcontroller for connecting the first UART to at least one of the first microprocessor and the second UART, respectively based on detecting the predetermined signal.

30 9. The method of claim 7, wherein the switch mechanism is implemented as a hardware switch connecting the first UART to at least one of the

first microprocessor and the second UART, respectively based on detecting the predetermined signal.

10. The method of claim 7, wherein the switch mechanism is  
5 implemented partially in hardware and partially in software for connecting the first UART to at least one of the first microprocessor and the second UART, respectively based on detecting the predetermined signal.

11. A computing system comprising:  
10 a first chip comprising a first UART, a second UART, a switch mechanism and a first microcontroller, wherein the first UART is in communication with an external interface and the first UART is connectable to the second UART and the first microcontroller via the switch mechanism; and  
15 a second chip comprising a second microcontroller and a third UART connected between the second UART and the second microcontroller;  
wherein the switch mechanism causes data to be routed between the second microcontroller and the external interface via the first, second and third UARTs, in response to detecting a first logic level.

20 12. The computing system of claim 11, wherein the switch mechanism causes data to be routed between the external interface and the first microcontroller via the first UART, in response to detecting a second logic level.

25 13. The computing system of claim 11, wherein the switch mechanism is implemented in software.

14. The computing system of claim 11, wherein the switch mechanism is implemented in hardware.

30 15. The computing system of claim 11, wherein the switch mechanism is implemented in both software and hardware.

16. The computing system of claim 12, wherein the first and second logic levels have equal values.

5        17. A method for controlling data communications between an external interface and first and second chips, the first chip comprising first and second universal asynchronous receiver-transmitters (UARTs) and the second chip having a third UART, the method comprising:

10      monitoring signals communicated from the external interface to the first UART; and  
              routing data from the first UART to the third UART, via the second UARTs, in response to detecting a switch signal.

15      18. The method of claim 17, further comprising:  
              monitoring signals communicated from the third UART to the second UART; and  
              routing data from the third UART to the first UART, via the second UART, in response to detecting a switch signal.

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